

**IN THE CLAIMS**

Please amend the claims as follows:

1. (Original) A current source adapted to produce an output current comprising:  
first and second circuit branches connected between first and second reference voltages,  
the first branch including a branch resistor connected at a junction node to a compensation  
resistor which is connected to the second reference voltage; and  
a start-up circuit connected to generate a start-up current at the junction node whereby the  
voltage across the compensation resistor increases with the first reference voltage and acts to  
reduce changes in the output current with the first reference voltage.
2. (Original) A current source according to claim 1, wherein the first circuit branch  
comprises first and second series-connected bipolar transistors, the base of the first transistor  
being connected to its collector.
3. (Original) A current source according to claim 2, wherein the second circuit  
branch comprises third and fourth series-connected bipolar transistors, the third bipolar transistor  
being connected as a current mirror with the first bipolar transistor and the fourth bipolar  
transistor being connected as a current mirror with the second bipolar transistor.
4. (Presently Amended) A current source according to claim 2, ~~or 3~~, which  
comprises an output transistor having its base connected to the base of the first transistor, the  
collector current of the output transistor constituting the output current.
5. (Presently Amended) A current source according to claim 2, ~~3 or 4~~, wherein the  
branch resistor is connected between the junction node and the emitter of the second transistor.
6. (Presently Amended) A current source according to ~~any preceding claim~~, 1,

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wherein the start-up circuit comprises a pair of start-up transistors connected in a current mirror configuration and a start-up resistor connected between the collector of one of said start-up transistors and said junction node.

7. (Original) A current source according to claim 3, wherein the area of the second transistor is larger than the area of the fourth transistor.